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Concept of Implementing Optimized Finite Impulse Response (OFIR) Filter using UltraScale FPGA

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Abstract: The important issue in filter is the design in real-time. For that DSP is obvious choice. However, due to recent advancement in FPGA, it is worth to have the designing and optimization of filter in latest FPGA to produce faster results with more features in design prospective. In this work, the digital filter design and optimization is carried using latest FPGA in order to ease the complexity of design and accelerate the optimization of FPGA

Keywords: FPGA System Design, Filter Design, Optimization

1. Introduction

Filter design is the process of designing a signal processing filter that satisfies a set of requirements, some of which are contradictory. The purpose is to find a realization of the filter that meets each of the requirements to a sufficient degree to make it useful for various applications [1]. The filter design has certain requirements that need to be fulfill, these include, frequency response, impulse response, the filter stability and other design features. The frequency response defines the steepness and complexity of the response curve is a deciding factor for the filter order and feasibility [2]. A first-order recursive filter will only have a single frequency-dependent component. This means that the slope of the frequency response is limited to 6 dB per octave. One most important point to design filter is accompanying weighting function, which describes, for each frequency, how important it is that the resulting frequency function approximates the desired one. The larger weight, the more important is a close approximation [3]. The filter is characterized in different types such as, low-pass, high-pass, bandpass and many more [4].

In addition, there is impulse response that may be the filter's impulse response that is explicit and the design process then aims at producing as close an approximation as possible to the requested impulse response given all other requirements [4]. In some cases it may even be relevant to consider a frequency function and impulse response of the filter which are chosen independently

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from each other. For example, we may want both a specific frequency function of the filter and that the resulting filter have a small effective width in the signal domain as possible. The goal of the design process is then to realize a filter which tries to meet both these contradicting design goals as much as possible. The important aspect of filter design is Computational complexity that is any design is that the number of operations (additions and multiplications) needed to compute the filter response is as low as possible. In certain applications, this desire is a strict requirement, for example due to limited computational resources, limited power resources, or limited time [5]. The last limitation is typical in real-time applications. For discrete filters the computational complexity is more or less proportional to the number of filter coefficients. If the filter has many coefficients, for example in the case of multidimensional signals such as tomography data, it may be relevant to reduce the number of coefficients by removing those which are sufficiently close to zero.

Furthermore, the filter implementation is also important there are several ways in which it can be design such as Analog, Digital, Mechanical and etc [6]. In this work, the focus is on Digital Filter only because of wide application in electronics and communication. These are further divided in to Finite impulse response, or FIR, filters express each output sample as a weighted sum of the last N input samples, where N is the order of the filter. FIR filters are normally non-recursive, meaning they do not use feedback and as such are inherently stable. Infinite impulse response, or IIR, filters are the digital counterpart to analog filters. Such a filter contains internal state, and the output and the next internal state are determined by a linear combination of the previous inputs and outputs (in other words, they use feedback, which FIR filters normally do not). The optimization is also is in important factor [6].

Filter Optimization, can optimize mappings by filtering within a customized data object and by placing filters early in the mapping. Use a filter in a customized data object to remove the rows at the source. If you filter rows from the mapping, you can improve efficiency by filtering early in the data flow. Use a filter in a customized data object to remove the rows at the source. The customized data object limits the row set extracted from a relational source. If you cannot use a filter in the customized data object, use a Filter transformation and move it as close to the customized data object as possible to remove unnecessary data early in the data flow. The Filter transformation limits the row set sent to a target. Use a filter in an Update Strategy transformation if you do not need to keep rejected rows. To improve mapping performance, you can also use a Filter transformation to drop rejected rows from an Update Strategy transformation if you do not need to keep rejected rows. Avoid complex expressions in filter conditions. Avoid using complex expressions in filter conditions. To optimize Filter transformations, use simple integer or true/false expressions in the filter condition. The Filter transformation filters data within a mapping. The Filter transformation filters rows from any type of source. The customized data object filters rows from relational sources. The Filter transformation filters rows from any type of source.

The important issue in filter is the design in real-time. For that DSP is obvious choice. However, due to recent advancement in FPGA, it is worth to have the designing and optimization of filter in latest FPGA to produce faster results with more features in design prospective. In this work, the digital filter design and optimization is carried using latest FPGA in order to ease the complexity of design and accelerate the optimization of FPGA.

2. Literature Review

In the past, the various studies have carried out related to filter design, filter design implementation in FPGA, optimization and etc. The related studies are discussed below.

[7] Zhao in 2016 proposed the unbiased finite impulse response filter by linking solution between the unbiased FIR filter and other types. The filter estimates to minimize the mean square error (MSE) subject to the unbiasedness constraint and then find its fast iterative form. Filter allows for ignoring system noise. The results presented in this paper no longer be considered to be at cross purposes because the Filter is shown to be a special case of the algorithm, which does not require the noise statistics. It also has much better robustness than the other filters. It allows for neglecting the process noise while still outperforming the common filter KF. There filter response is quite well, however struggling with Design concept in analog form, optimization feature is missing and furthermore, the design verification and validation was lagging in the work.

[8] Liu in 2015 presents the novel architectures for linear phase FIR digital filters using stochastic computing the system was design using logic gates that are inherently fault-tolerant and structures were created using nanoscale CMOS technologies. Compared to direct-form linear-phase FIR filters, linear-phase lattice filters require twice the number of multipliers but the same number of adders. The one of the main issues with system was hardware complexities of stochastic implementations of linear-phase FIR filters for direct-form and lattice structures are comparable. The system was designed using ICA '99 Synthetic Benchmarks. However, the error-to-signal power of stochastic directform or lattice filter is an order of magnitude higher at very low fault rates but is more than two orders of magnitude less when the fault rate is about one percent than the direct-form, where the faults represent random bit-flips at outputs of all logic gates. The issues with this work was hardware implementation and lack of optimizing feature.

[9] Pak J M in 2016 proposed a new filtering algorithm called the self-recovering algorithm. It diagnosed, an assisting filter, a nonlinear finite impulse response (FIR) filter. The performance of the proposed filter are demonstrated through two applications–the frequency estimation and the indoor human localization. The filter has aan ability to self-recover from failures during the state estimation process. The effectiveness and performance of the filter were shown by the two applications–frequency estimation and indoor human localization. The process noise was inappropriate. The work planned to apply the filter to various tracking problems that use the random-walk motion model. The system has degraded performance in terms of optimization and real-time implementation was challenging.

[10] Bhaskar in 2016 improved the capacity and performance and a decrease in cost, FPGAs have become a viable solution for making custom chips and programmable DSP devices. This paper presents an efficient implementation of Finite Impulse Response Filter (FIR) using Distributed Arithmetic (DA) architecture based on FPGA with the help of Xilinx system generator software. Here, the multipliers in FIR filter are replaced with multiplier to remove high frequency noise from ECG signal. The work proposed that the signals under experiment has been added with muscle noise and after applying different FIR method, the signals according to signal noise ratio (SNR) and MSE (mean square error) are evaluated. The data was carried from Massachusetts Institute of Technology University and Beth Israel Hospital (MIT-BIH) database. The implementation is done on a Xilinx chip of Spartan 3E XC3S500e-4fg320 using Xilinx system generator 10.1 with Matlab version7.4.0 (2007a). The designed

low pass FIR filter with Kaiser Window works excellent in removing High frequency. It has been deduced that utilization of hardware resources using DA FIR has been minimized. The issues with system was attention needs to pay for reduction in leakage power as a VLSI backend activity, where near about 90 % power is leakage power. The real-time implementation was slow and filter optimization was not performed for the filter.

[11] Anmin H in 2016 compared the linear phase frequency characteristic of Infinite Impulse Response(IIR) digital filter, Finite Impulse Response(FIR) digital filter not only ensures the accurate strict linear phase characteristic, simple structure and stable in the design and application of digital filter. But the FIR need higher order when complete the same design index, this paper proposes an improved distributed algorithm in order to meet the design of high-speed and high-order digital FIR filter. The algorithm uses the Polyphase decomposition and pipeline technology and multiplexing adder pre-add the data to reduce the Look up Table(LUT) size of the traditional distribute algorithm of mainstream Field Programmable Gate Array (FPGA) chip. The paper makes use of Matlab simulation design, Quartus II compile testing and downloads to the Field Programmable Gate Array(FPGA) to analysis, the results show that the method effectively reduces the filter to the consumption of hardware resources, can realize the high-order FIR filter in a more appropriate way. The filter was not well designed based on characterization in terms of filter coefficients, precession fractional lengths and etc. furthermore, the optimization feature was not focused in the work.

[12] Szadkowski Z in 2016 developed a new approach to a filtering of radio frequency interference (RFI). The linear equations were solved either in the virtual soft-core NIOS® processor (implemented in the FPGA chip as a net of logic elements) or in the external Voipac PXA270M ARM processor. Tests showed very good efficiency of the RFI suppression for stationary contaminations. However, we observed short-time contaminations, which could not be suppressed either by the IIRnotch filter or by the FIR filter based on the linear predictions. For the LP FIR filter, the refresh time of the filter coefficients was too long and the filter did not keep up with the changes in the contamination structure, mainly due to a long calculation time in a slow processors. First results in the laboratory are very promising. The linear predictor is an adaptive filter, but it has a limitation in its adaptation. The result of the simulations show that the LP filter works fine if the refreshment time of the coefficients is lower than the time of changes in the signal. The system was developed using FPGA but system performance is slow and optimization was not carried out.

[13] Alawad M in 2015 presented a hardware- and energy-efficient approach to implement FIR filtering through reconfigurable stochastic computing. The work presented for performing FIR filtering applicable in a wide range of DSP applications, where the requirement of absolute processing accuracy can be slightly relaxed. Our new multiplierless approach has two distinctive advantages when compared with the conventional multiplier-based or DA-based FIR filtering methods. First, it is especially effective for high-order FIR filtering because it bypasses costly multiplications and does not rely on large size of memory to store pre-computed coefficient products. Second, this new architecture is significantly more robust or fault tolerant than the conventional architecture because all signal values will be represented and computed probabilistically, and local signal corruption can not easily destroy the overall probabilistic patterns, therefore achieving much higher error tolerance. The main issues with the filter was real-time implementation was not performed.

[14] Sun Chao in 2020 designed by the analog circuit the implementation was carried out on FPGA. This paper mainly explains the FIR filter principle and filter coefficient calculation, and simulates the linear filter with the sampling rate of 1Mhz, the passband is 120Khz, and the order is 15th order. Finally, the experimental verification is carried out through the FPGA board, and the corresponding design. The system was designed using low parameters without optimization.
[15] Wang Xinin 2019 in Field Programmable Gate Array (FPGA) devices are widely used in the field of Digital Signal Processing (DSP), and the algorithm of DSP has been used in many fields such as speech signal processing, audio signal processing, image processing, information system, control system and so on. In the development and design of modern digital systems, the use of programmable logic devices is becoming more and more common. There are many ways to implement signal processing algorithm based on FPGA: the first one is to design with VHDL or Verilog HDL language; the second one is to use mature IP core encapsulated by FPGA company; the third one is to design with.
[16] Zheng in 2018 designed the FIR filter using FPGA via DSP real time chip via PLD devices. The system was designed using ModelSim with limited capabilities. The key features of the work was development of Low pass filter using DSP. The system design lacking in slow time with no optimization features.
[17] S. Rengaprakash in 2017 designed using the concepts of polyphase decomposition to provide the speed benefit. In this paper, hardware implementation of fast running FIR filter on a Virtex-5 FPGA is proposed and the design is compared with two different techniques: FIR filter design using optimized transpose structure and FIR filter design using Distributed Arithmetic (DA) approach. The fast running FIR filter designed in this paper is two times faster than the usual FIR filter. The optimization of the filter was not carried out.
[18] Cui Guo-wei in 2013 implemented multiply-add structure, DA has the characteristics of parallel data processing and efficient operation. The design of FPGA has practical applications in digital signal processing; it has certain directive significance to the reform of electronic technology practice teaching. According to the low pass filter in this paper, we can get high pass or band pass filter through by simply recombining filter characteristic parameters. At the same time, basing on the programmable nature of FPGA devices, the circuit is conveniently improved, which further improve the easy circuit performance.

3. Methodology

The Objectives of this work is Design the HDL design Optimized FIR Low-pass Filter, Analyze the HDL based designed Optimized FIR Low-pass Filter and Verify and validate the designed Optimized FIR Low-pass Filter using UltraScale FPGA.

4. Concept and plan of work

In this research work a HDL based Optimized FIR Low-pass Filter is proposed in order to enhance the performance of filter in terms of speed, power and design features. The Fig. 1 discusses the Methodology of Proposed. The proposed system will be developed using MATLAB and Xilinx ISE for implementation in FPGA.

Fig 1 – Proposed Methodology

The proposed methodology of designing the optimized HDL filter using FPGA will be carried out using different design step. In the first step, the Low-pass FIR filter design will be created using MATLAB via FDA Tool using Response Type, Design Method, Filter Order, Frequency and Magnitude Specifications, after that filter quantization will be performed in order to convert in digital domain.

In the second step, the HDL based filter design will be developed using VHDL code. This will require to configure input and output ports, clock setup, IO Standards, and after that verification of HDL based of low-pass optimized low pass filter will be simulated. In the third step, the verified vhdl code will be implemented in Xilinx ISE in order to create the real-time architecture for design the filter in FPGA. In the fourth step, timing analysis will be performed for developed HDL based optimized low-pass FIR filter. In the final step, the design step will be given to FPGA for real-time implementation as shown in Fig.2.

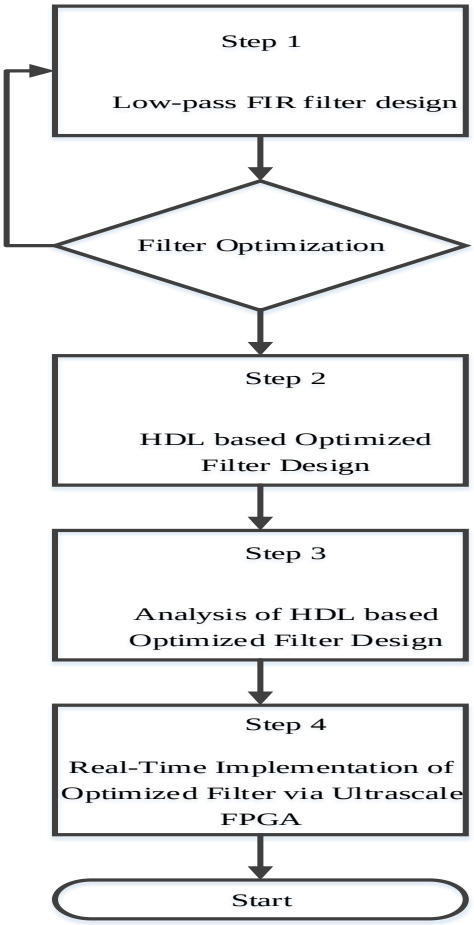

Fig 2 – Research Work Flow

5. Outputs

The research work proposed the optimized HDL based filter design approach in FPGA for configuring the filter for better performance in terms of speed, timing analysis. The designed filter can be used in different industrial application to optimize speed of controllers and remove noise from various Electronic and Communication Circuits. The proposed model will be helpful for various applications.

6. Utilization of Results

Suitable outcomes would be reported in the form real-time implementation and results will be published in the form papers and thesis.

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